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U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
VIXS.0100300 (1459-0100300)

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on May 24, 2006

Signature Jennifer Jensen

Typed or printed name Jennifer Jensen

Application Number	Filed
09/995,308	November 27, 2001

First Named Inventor: Paul DUCHARME

Art Unit	Examiner
2131	Shin Hon CHEN

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☐ attorney or agent of record. Registration number _____
- ☑ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 51,596

Signature

Ryan S. Davidson
Typed or printed name

512-439-7100
Telephone number

24 May 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Paul DUCHARME		
Title:	A MONOLITHIC SEMICONDUCTOR DEVICE FOR PREVENTING EXTERNAL ACCESS TO AN ENCRYPTION KEY		
App. No.:	09/995,308	Filed:	11/27/2001
Examiner:	CHEN, Shin Hon	Group Art Unit:	2131
Customer No.:	29331	Confirmation No.:	9477
Atty. Dkt. No.:	VIXS.0100300 (1459-0100300)		

Mail Stop AF
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

REMARKS IN SUPPORT OF THE PRE-APPEAL BRIEF REQUEST FOR REVIEW

Dear Sir:

In response to the Final Office Action mailed January 24, 2006 (hereinafter, "the Final Action") and the Advisory Action mailed March 14, 2006 (hereinafter, "the Advisory Action") and pursuant to the Notice of Appeal and Pre-Appeal Brief Request for Review submitted herewith, the Applicant requests review of the following issues on appeal.

Easter and Van Oorschot fail to disclose a silicon die pad having an input coupled to the output port of a memory location to provide temporary access as recited by claims 1 and 41

Independent claim 1 presently recites the features of a memory location having an output port, wherein a data value to be stored in said memory location is observable only internally to the monolithic semiconductor device, and at least one silicon die pad having an input coupled to the output port of said memory location to provide temporary access to said memory location. Independent claim 41 recites similar features. The Office asserts the key array 25/fuse array 51 of Easter discloses the claimed memory location feature and, in the Final Action, that Figure 2 of

Easter and the passage of Easter at column 4, lines 50-65 disclose the claimed silicon die pad feature. As noted at pages 6 and 7 of the Response to the Final Action mailed March 24, 2006 (hereinafter, "the Final Response"), Easter fails to disclose or even suggest any silicon die pads, much less a silicon die pad having an input coupled to the output port of a memory location to provide temporary access to the memory location as recited by claim 1. In response, the Advisory Action asserts "the integrated circuits are well known in the art to contain die pads." *Advisory Action*, p. 9. While the Applicant does not disagree with the proposition that integrated circuits are well known to contain die pads, the Office errs in the unreasonable extension of this general statement to conclude that it is well known to use silicon die pads that have an input connected to an output port of a memory location to provide temporary access to the memory location. To wit, the Office has failed to provide any reference that demonstrates that it is well known to connect the input of a silicon die pad to the output port of a memory location to provide temporary access to the memory location. Further, it is submitted that it is not in fact well known to use a silicon die pad in this manner. As the Office fails to provide any evidence to the contrary, the Office has failed to meet its burden in establishing a *prima facie* case of obviousness for claims 1 and 41 and their dependent claims.

Easter and Van Oorschot fail to disclose generating a first encryption key based on data from a memory location and providing the first encryption key for storage in the memory location as recited by claim 33

Independent claim 33 presently recites the features of: accessing, by a first encryption engine internal to a monolithic semiconductor device, data from a memory location internal to the monolithic semiconductor device, wherein the memory location is accessible only internal to the monolithic semiconductor device; generating, at the first encryption engine, a first encryption key based on the data from the memory location, wherein the data represents a second encryption key; and providing the first encryption key for storage in the memory location. The Final Action asserts that the key array 25/fuse array 51 of Easter discloses the claimed memory location feature, the RSA engine 57 of Easter discloses the claimed first encryption engine feature, and that Figure 5 of Easter and the passage of Easter at col. 8, lines 18-26 disclose the claimed feature of providing the first encryption key (generated by the first encryption device) for storage in the memory location. The Advisory Action elaborates by asserting that the passage of Easter at col. 8, lines 18-26 disclose "the public key engine is used to generate the key required by the

DES engine and the key is stored in the key array." *Advisory Action*, p. 9. For ease of reference, the cited passage of Easter is reproduced in its entirety:

> Keys for DES encryption engine 21 are stored in key array 25. This is a programmable storage area comprising, for example, RAM. Operationally, keys are transferred for use as DES master keys via public key cryptography techniques using RSA engine 57. One technique for such transfer is described in Munck et al., incorporated by reference hereinabove. Advantageously, using the techniques of the present invention, the private key is secured and the disadvantages of prior manual key loading systems are overcome.

Easter, col. 8, lines 18-26 (emphasis added).

Thus, assuming, *arguendo*, that the key array 25/fuse array 51 is equivalent to the claimed memory location feature, the RSA engine 57 is equivalent to the claimed first encryption engine feature, Easter would have to disclose or suggest that an encryption key generated by the RSA engine 57 is stored in the key array 25/fuse array 51 to be consistent with the claimed feature of providing the first encryption key for storage in the memory location. However, contrary to the assertions of the Final Action and the Advisory Action, Easter fails to disclose or suggest this feature. As will be appreciated, the cited passage of Easter reproduced above fails to disclose or suggest that any encryption keys generated by the RSA engine 57 are stored in the key array 25/fuse array 51. Rather, this cited passage merely provides that "keys are transferred for use as DES master keys via public key cryptography techniques using RSA engine 57. One technique for such transfer is described in Munck, et al. . . . " *Id.* However, this statement does not imply that the keys are transferred via the key array 25/fuse array 51. Rather, turning to Figure 5 of Easter, Easter illustrates that the connection between the key array 25/fuse array 51 as a unidirectional arrow from the key array 25/fuse array 51 to the RSA engine 57, and Easter does not provide any indication that the connection is bidirectional from the RSA engine 57 to the key array 25/fuse array 51. Further, Figure 5 illustrates that the only output of the RSA engine 57 is connected to the buses 35 and 35' and that the only input to the DES engine 21 is via the busses 35 and 35'. Further Figure 5 fails to illustrate that the output of the RSA engine 57 is connected to an input of the key array 25/fuse array 51 in any manner. In fact, Figure 5 fails to illustrate any input to the key array 25/fuse array 51. Thus, in view of Figure 5 of Easter and the corresponding disclosure of Easter, one of ordinary skill in the art would appreciate that

the RSA engine 57 is connected to the DES engine 21 via the busses 35 and 35' and would not interpret Easter as disclosing or suggesting that an encryption key output by the RSA engine 57 is provided for storage in the key array 25/fuse array 51.

There is no motivation to modify the teachings of Easter and Van Oorschot in view of the teachings of Pitts with respect to claim 17

Independent claim 17 recites the features of an external data port having an input and an output, a memory location having an output coupled to an input of a first encryption engine, and an isolation portion coupled to the output of said memory location and to the input of said external data port, wherein said isolation portion is modifiable to permanently prevent access of said memory location by the external data port. The Final Action acknowledges that Easter and Van Oorschot fail to disclose the claimed isolation portion feature. The Final Action therefore relies on Pitts as disclosing an isolation fuse element that enforces one time programming of the memory. *Final Action*, p. 9. The Final Action therefore asserts that it would have been obvious "to include a fuse element in the semiconductor device [of Easter] because [a] semiconductor device with [a] fuse is well known in the art. Therefore it would have been obvious . . . to combine the teachings of Pitts within the system of Easter because it prevents external access to the memory location after data has been successfully stored into secure memory array." *Id.*

In contrast with the assertions of the Final Action, it is respectfully submitted that one of ordinary skill in the art would not be motivated to combine the teachings of Easter and Pitts as proposed. As noted by the Final Action, Pitts discloses a technique for preventing *external* access to a memory array 108 via the *external* data path 118 of the circuit 100 by implementing an AND gate 110 and fuse element 112 in the external data path 118. *See, e.g., Pitts*, FIG. 1. However, Easter does not disclose that the key array 25/fuse array 51 (which would be analogous to the memory 108 of Pitts) is connected to or accessible an *external* data path of the IC chip 63. Further, Easter provides no indication that the connection of the key array 25/fuse array 51 to an *external* data path of the IC chip 63 would be desirable or advantageous in any way. Thus, as Pitts discloses the use of an AND gate 110 and a fuse 112 to prevent external access to a memory array and as Easter fails to disclose an *external* data path that accesses the key array 25/fuse array 118 in which the AND gate 110 and the fuse 112 of Pitts can be implemented, one of ordinary skill in the art would find no motivation to utilize the AND gate 110 and fuse element

112 taught by Pitts in the circuit of Easter. As there is no motivation to combine the teachings of Easter and Pitts as proposed by the Office Action, the Office Action fails to establish a *prima facie* case of obviousness for claim 17.

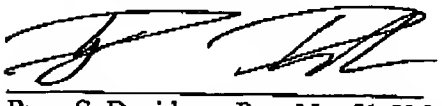
New grounds of rejection for claims 1 and 41 in Advisory Action improper

As noted above, the Advisory Action responded to the Applicant's notice that Easter fails to disclose the claimed silicon die pad feature of claims 1 and 41 by asserting "the integrated circuits are well known in the art to contain die pads." *Advisory Action*, p. 9. Thus, the Advisory Action sets forth a de facto "Official Notice," and the Advisory Action therefore in actuality is rejecting claims 1 and 41 under the combination of Easter, Van Oorschot, and the Examiner's "Official Notice," which is a different grounds for rejection than the combination of solely Easter and Van Oorschot as set forth in the Final Action. As the Advisory Action raises new grounds of rejection not present in the Final Action, the Advisory Action is improper and the Office should issue a new Office Action should claims 1 and 41 continue to be rejected even in view of the above remarks so that the Applicant can more fully consider and respond to the Examiner's Official Notice.

Conclusion

As discussed above, the Final Action and Advisory Action fail to establish that the proposed combinations of the cited references disclose or suggest each and every element recited by any of the pending claims. Accordingly, reconsideration and withdrawal of these rejections is respectfully requested.

Respectfully submitted,



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24 May 2006
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